The expansion hardware provides additional memory and communication capabilities for the AT&T UNIX PC. The expansion hardware's EIA ports make it possible for the PC to communicate with another terminal or computer. Additional memory and EIA capabilities are available separately or in combination, as shown in the following list of expansion hardware options:

- 0.5MB RAM Expansion Board (no EIA ports)
- 2.0MB RAM Expansion Board (no EIA ports)
- 0.5MB EIA/RAM Combo Board (two EIA ports)
- 1.0MB EIA/RAM Combo Board (two EIA ports)
- 1.5MB EIA/RAM Combo Board (two EIA ports)
- Dual EIA Port Board (no RAM, two EIA ports)

The expansion hardware includes:

- An interface connection P1 and associated circuitry
- RAM memory
- EIA connection circuitry (if an EIA or Combo board)

Interface Circuitry

All communications between the expansion board and the **UNIX** PC bus are through the expansion board interface connector P1.

Input/Output Handling

As a direct memory access (DMA) device, data transfer from the expansion board to the PC bus causes the 68010 to wait while data is transferred into RAM memory. Data transfer is considered a fast cycle (500 ns).

There are three functions which the expansion board may be called upon to perform. Read to memory, read from memory and port to or from memory to the RS-232 interface.

Expansion Board Schematic

Sheet 2--Memory Access Control Circuitry:

This circuitry consists of address latch 1K, lower and upper data strobe control, consisting of demultiplexers 3H and 3J and OR gates 3B and parity interrupt, 2C and 2E.

Sheet 3--Memory Bus Management and Communications Circuitry:

The upper portion of sheet 3 of the schematic contains map address management circuitry consisting of multiplexers 4A, 4B, 4C, 4E, 4H, and 4J. The lower portion of sheet 3 contains the communication interface IC 11E, RS-232 line drivers 12J, 12K, and 12A, and RS-232 receivers 11A and 12B and port connectors J1 and J2.

Note

This circuitry is present only on the EIA/RAM Combo and EIA/RAM boards. The 0.5 and 2.0 RAM expansion boards do not contain interface circuitry or RS-232 ports.

Sheets 4, 5 and 6--Memory (RAM):

Memory circuitry consists of the X, Y, and Z bus, the read bus and read bus control 11H and 11C, and upper and lower parity generator ICs 5K through 10K.

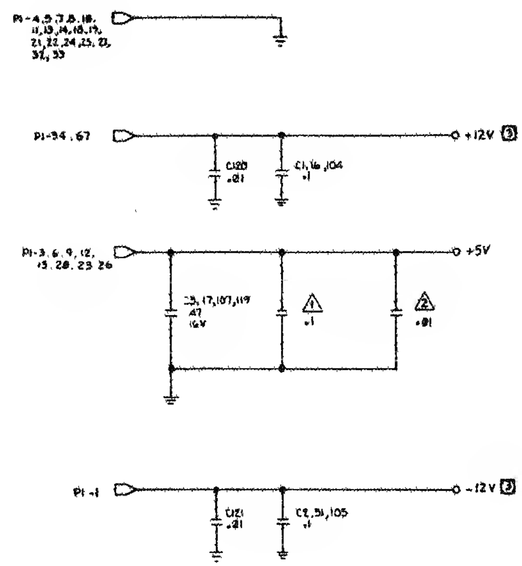
Depending on the amount of RAM that is mounted physically on the expansion board, these locations may or may not be used.

Sheet 5--Expansion Bus Interface:

The lower portion of sheet 5 of the schematic also contains data transceivers 1C and 1E connected to the read bus and expansion bus connector P1 completing the expansion loop.

REVISIONS					
ZONE	REV	DESCRIPTION	DATE	DWN	APPROVED
	A	RELEASE TO CONTROL	[illegible]	[illegible]	[illegible]
	B	REVISED PER C.O. # 5190	[illegible]	[illegible]	[illegible]
	C	REVISED PER CO # 5203	[illegible]	[illegible]	[illegible]
	D	REVISED PER CO # 5201	[illegible]	[illegible]	[illegible]
	DI	PER RECORD CHANGE # D-025	[illegible]	[illegible]	[illegible]
	E	REVISED PER C.O. 6411	[illegible]	[illegible]	[illegible]
	F	REVISED PER C.O. # 5346	[illegible]	[illegible]	[illegible]
	G	REVISED PER C.O. # 5446	[illegible]	[illegible]	[illegible]

I.C. DEVICE CHART				
I.C TYPE	REFERENCE DESIGNATIONS	+5V	GND	UNUSED OUTPUTS
74F00	2A, 2H	14	7	
74F08	3A, 1H	14	7	
74F32	3B, 2J	14	7	
74AS74	1B	14	7	
74F138	3E, 3H, 3J	16	8	
74F245	1C, 1E	20	10	
74F258	4A, 4B, 4C, 4E, 4H, 4J, 3K, 4K	16	8	
74F373	1K	20	10	
74F85	1J	16	8	
74LS125	1A, 11B	14	7	
82S123	11H	16	8	
74LS280	2C, 2E	14	7	
1488	12A, 12J	3	7	
1489	11A, 12B, 12K	14	7	
8530	11E	9	31	
48256	5A, 5B, 5C, 5D, 5E, 5F, 5H, 5J, 5K, 6A, 6B, 6C, 6D, 6E, 6F, 6H, 6J, 6K, 7A, 7B, 7C, 7D, 7E, 7F, 7H, 7J, 7K, 8A, 8B, 8C, 8D, 8E, 8F, 8H, 8J, 8K, 9A, 9B, 9C, 9D, 9E, 9F, 9H, 9J, 9K, 10A, 10B, 10C, 10D, 10E, 10F, 10H, 10J, 10K	8	16	
74F86	2B	14	7	
74123	2K, 11K	16	8	
74LS374	11C	20	10	
DL	3C	14	7	



1 C4, 6, 8, 11, 13, 15, 20, 21, 22, 23, 25, 27, 29, 30, 41, 43, 45, 47, 48, 51, 53, 55, 57, 60, 61, 62, 64, 66, 68, 69, 71, 73, 75, 77, 80, 82, 84, 94, 95, 97, 98-100, 92, 112, 114, 116, 118

2 C5, 7, 10, 12, 14, 19, 24, 26, 28, 42, 44, 46, 49, 50, 52, 54, 56-58, 63-65, 67, 70, 72, 74, 76, 78, 81, 83, 85, 96, 99, 101, 103, 106, 111, 113, 115, 117

D - GO - 00221 - XX REV X

- D — DIVISION I.D.
- GO — IDENTIFIES AS PCA
- 00221 — BASIC PART NUMBER
- XX — VERSION NUMBER

4 PARTS AFFECTED BY VERSION

ASSY DASH NO.	VERSION CHARACTERISTIC	W1	W2	5A THRU 5K	6A THRU 6K	7A THRU 7K	8A THRU 8K	9A THRU 9K	10A THRU 10K	R3	R8		
-00	GENERIC												
-01	.5 MBYTE	—	INSTALL	INSTALL	INSTALL	—	—	—	—	—	—		
-02	1.0 MBYTE	INSTALL	—	—	—	INSTALL	INSTALL	INSTALL	INSTALL	—	—		
-03	1.5 MBYTE	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	INSTALL	—	—		

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. CONNECT PIN 14 OF ALL 1488'S TO +12V
   CONNECT PIN 1 OF ALL 1488'S TO -12V
4. PART AFFECTED BY VERSION; SEE TABLE
5. PAGE REFERENCE SHOWN AS:
   SHEET NO.
   ZONE

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	USED BUT NOT STUFFED
C123	C9, C37, C79	C18
J2		
P1		
R10		
RP12		
Y2		
W3		

SPARES (EXCL IC'S)	
PART	UNUSED PINS
RP6	1,2
RP7	1,2
RP9	1,2
RP11	3,4,5,6
J1	1, 9, 10, 11, 12, 13, 14, 16, 18, 19, 21, 22, 23
J2	1, 9, 10, 11, 12, 13, 14, 16, 18, 19, 21, 22, 23
P1	16, 17, 40, 42, 43, 44, 45, 54, 55, 59, 60, 61, 62, 63, 69, 71, 73

INCHES

THIRD ANGLE PROJECTION

Convergent Technologies

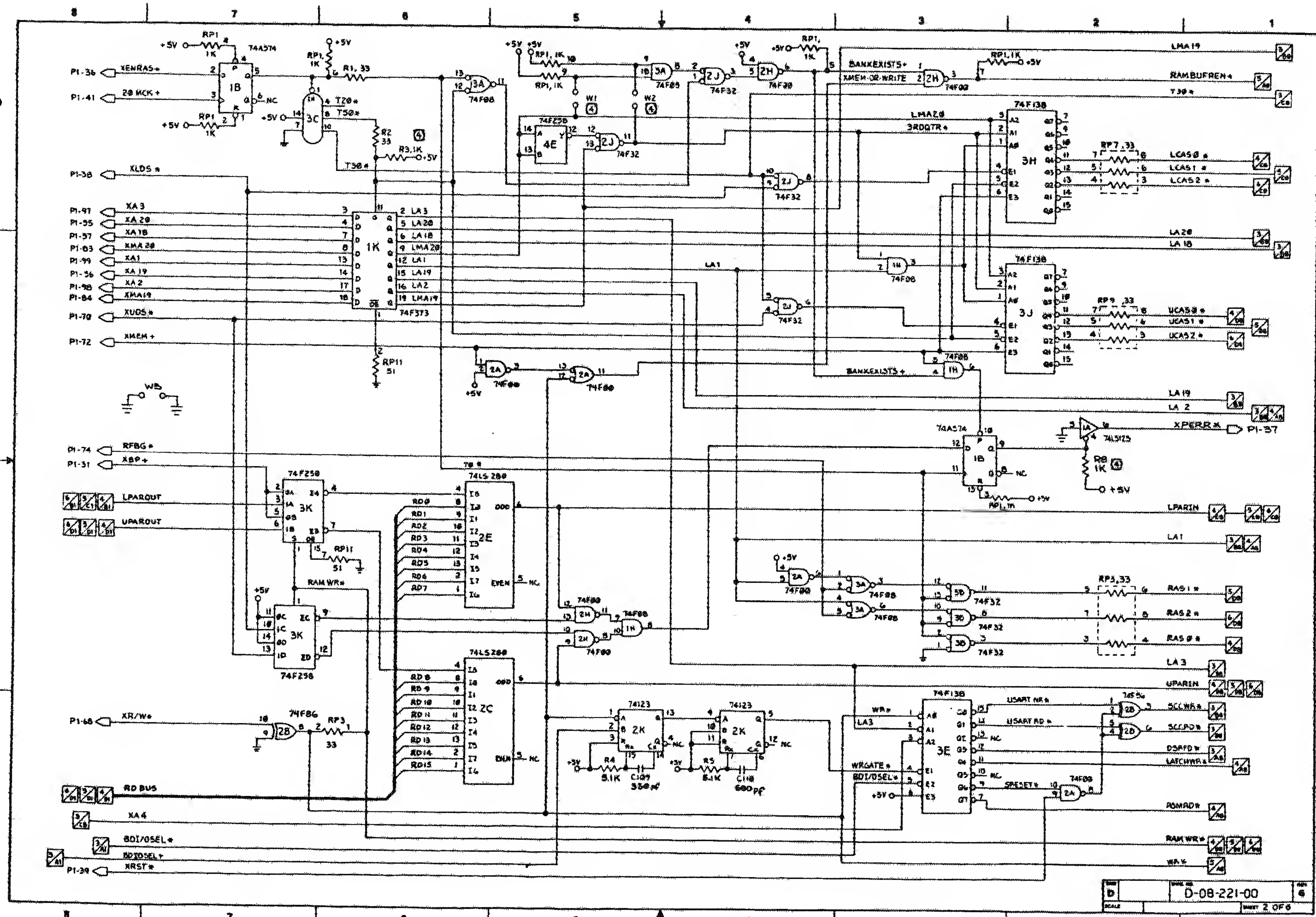
SCHEMATIC,
34 COMBO CARD

D | D-08-00221-00 | G

SHEET 1 OF 6

DO NOT SCALE DRAWING

APPLICATION



P1-36 XENRAS*
P1-41 20 MCK+
P1-38 XLDS*
P1-97 XA3
P1-55 XA20
P1-57 XA18
P1-83 XMA20
P1-99 XA1
P1-56 XA19
P1-98 XA2
P1-84 XMA19
P1-70 XUDS*
P1-72 XMEM+
P1-74 RFBG*
P1-31 XBP+
LPAROUT
UPAROUT
P1-68 XR/W*
RD BUS
XA4
BDI/OSEL*
BDIOSEL+
P1-39 XRST*
74AS74
74F373
74F258
74LS280
74F138
74F32
74F08
74F00
74123
74F86
74LS125
BANKEXISTS+
XMEM-OR-WRITE
LMA20
3RDQTR*
LMA19
RAMBUFREN*
T30*
LCAS0*
LCAS1*
LCAS2*
LA20
LA18
UCAS0*
UCAS1*
UCAS2*
LA19
LA 2
XPERR*
P1-37
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LA1
RAS1*
RAS2*
RAS0*
LA3
UPARIN
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USART RD*
SCCWR*
SCCRD*
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WRGATE*
SPESET*
ROMRD*
RAM WR*
WR*
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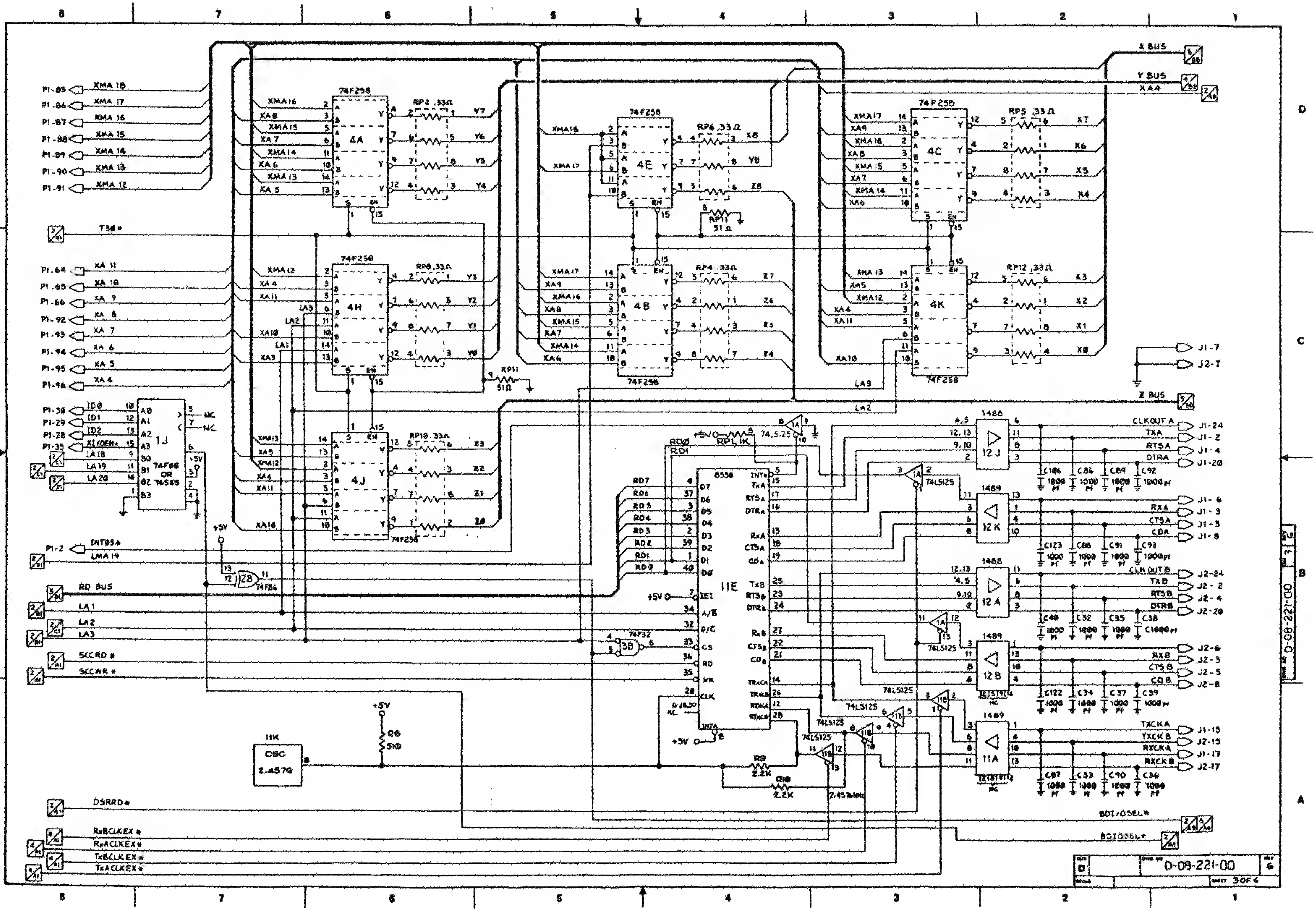
74F258
4A
4H
4J
4E
4B
4C
4K
1J
74F85 OR 74S85
11E
8530
1488
1489
12J
12K
12A
12B
11A
74LS125
74F32
74F86
11K
OSC 2.457G
X BUS
Y BUS
Z BUS
RD BUS
T30*
INTB5*
LMA 19
LA1
LA2
LA3
SCCRD*
SCCWR*
DSRRD*
RxBCLKEX*
RxACLKEX*
TxBCLKEX*
TxACLKEX*
BDI/OSEL*
BDIOSEL*
CLKOUT A
TXA
RTSA
DTRA
RXA
CTSA
CDA
CLKOUT B
TXB
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RXB
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CDB
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TXCKB
RXCKA
RXCKB
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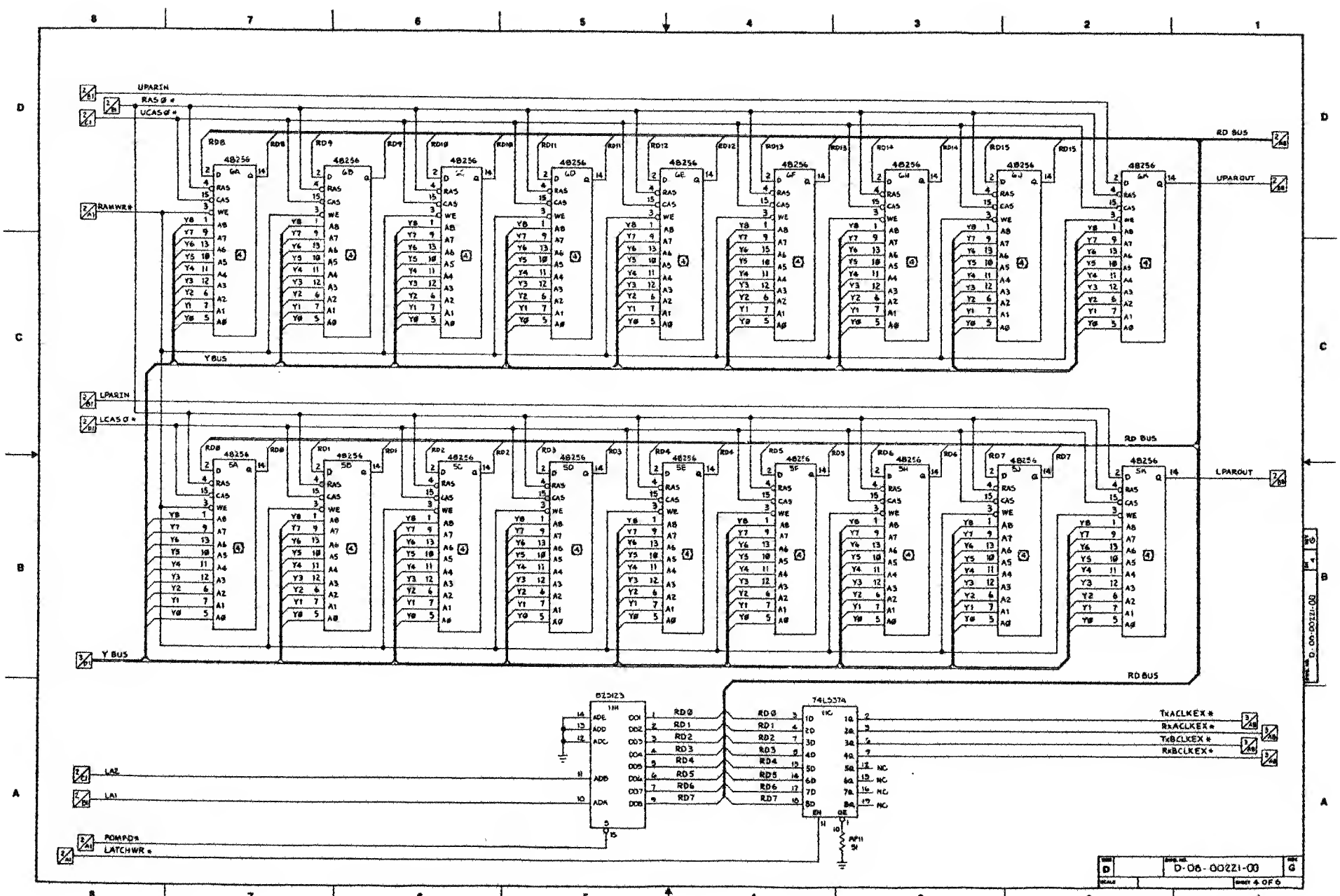
3 OF 6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UCAS Ø *
RAMWR*
YBUS
LPARIN
LCAS Ø *
Y BUS
RD BUS
UPAROUT
LPAROUT
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74LS374
82S123
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LATCHWR *
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RxACLKEX *
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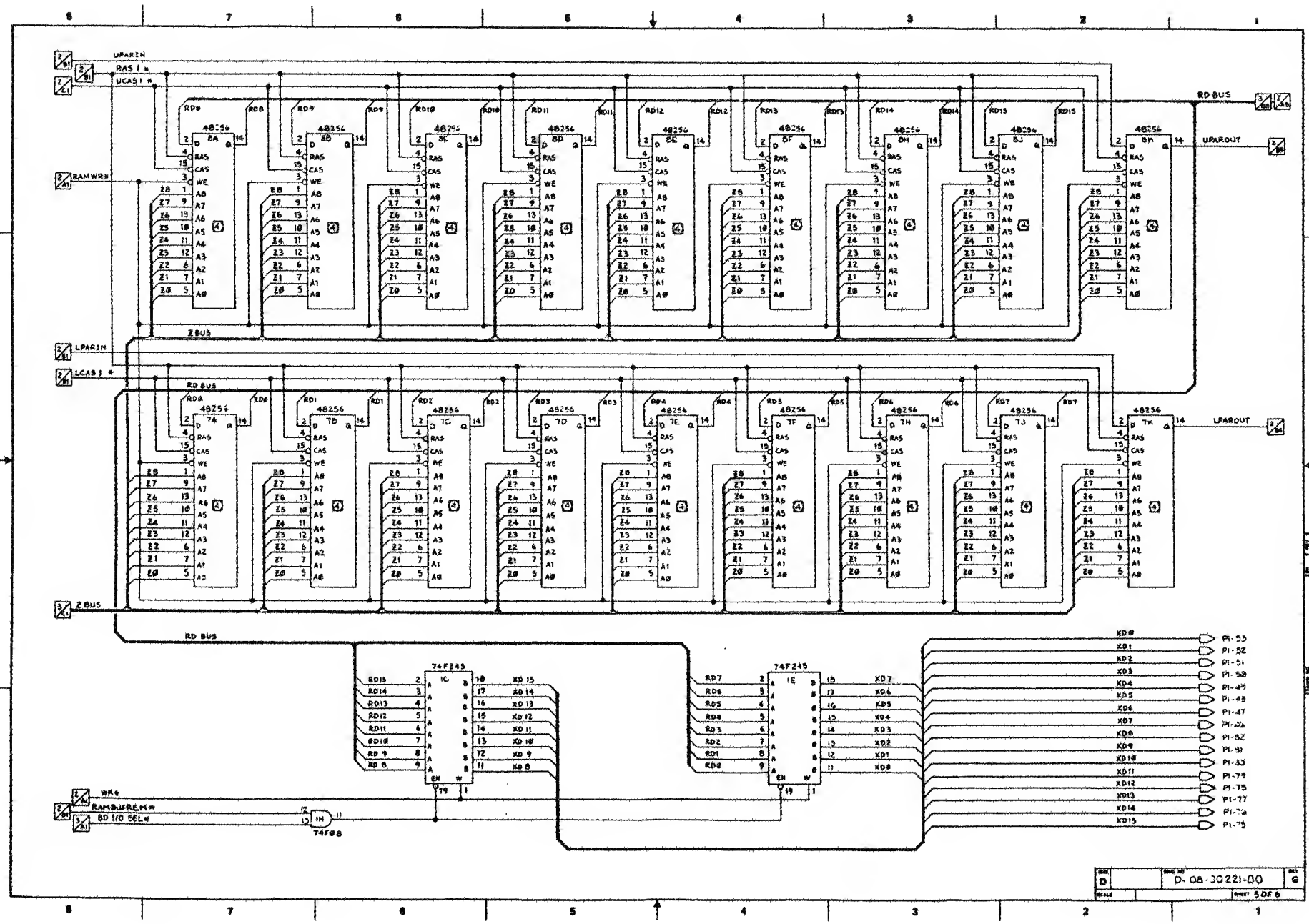
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ZBUS
UPAROUT
LPARIN
LCAS1*
LPAROUT
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WR*
RAMBUFREN*
BD I/O SEL*
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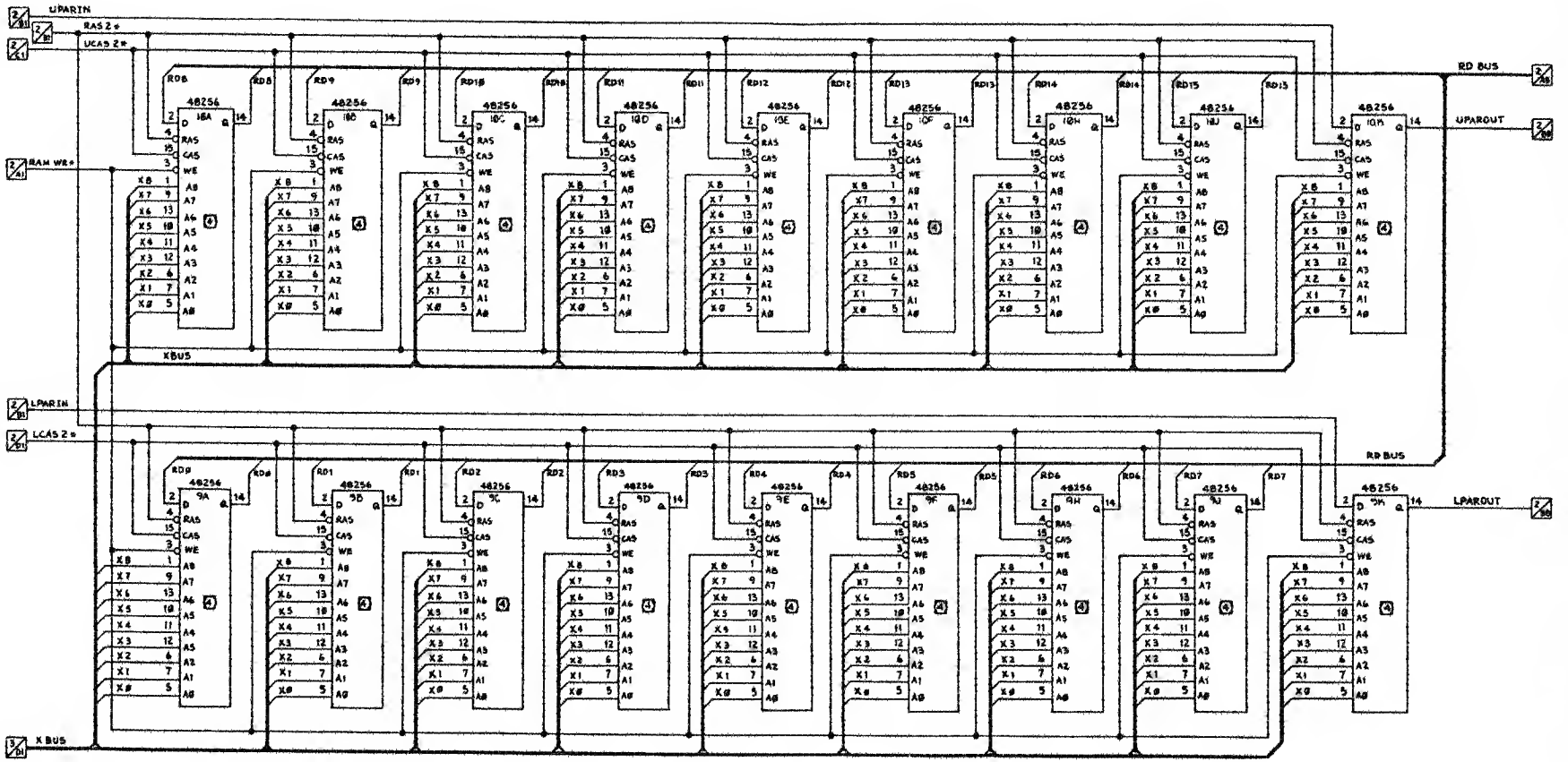
SHT 5 OF 6


UPARIN
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UCAS 2*
RAM WR*
XBUS
LPARIN
LCAS 2*
X BUS
RD BUS
UPAROUT
RR BUS
LPAROUT
48256
RAS
CAS
WE
D
Q
A0
A1
A2
A3
A4
A5
A6
A7
A8